Jason Lau

(929) 273-1217 | i@jasonlau.io | github.com/dotkrnl

EDUCATION

Ph.D. Computer Science — University of California, Los Angeles 2018 – 2024, Major GPA 4.0/4.0

Advisor: Prof. Jason Cong

B.Eng. Computer Science — Tsinghua University 2014 – 2018, Major GPA 93/100

B.A. Digital Media Arts — Tsinghua University, Academy of Arts & Design 2015 – 2018, Major GPA 88/100

Exchange Student — Hong Kong University of Science and Technology 2016 – 2017, Major GPA 4.0/4.0

PROFESSIONAL EXPERIENCE

Hardware Engineer — Jump Trading Group Aug 2025 – Present | Sunnyvale, CA

Researching and developing high-level synthesis algorithms for high-frequency trading, and creating high-performance FPGA and ARM hardware accelerators based on the developed toolchain. Developing low-latency hardware logic and integration for modern multi-die FPGAs to optimize trading performance.

Chief Technology Officer & Co-Founder — RapidStream Design Automation (Acquired by a Leading Global HFT Firm) Jan 2023 – Aug 2025 | Sunnyvale, CA

Devise the technical strategy and development of compiler solutions that deliver low-latency, high-performance FPGA accelerators. Engineered systems enabling efficient high-level physical designs directly from software specifications, significantly reducing compilation cycles.

Compilation Researcher (Intern) — Advanced Micro Devices (AMD), Xilinx Jun 2022 – Sep 2022 | Longmont, CO

Researched and implemented an MLIR compiler that is hardware physical aware for AMD Versal devices, targeting the AI Engine array. Designed flows enabling high-performance application acceleration on next-generation SoCs.

Cloud Software Engineer (Intern) — Google Jun 2016 – Sep 2016 | Cambridge, MA

Created "AwesomeChart," a cloud performance data analytical platform and visualization library capable of rendering millions of time series smoothly. The platform was integrated into Google Cloud Platform and remains in use by customers for monitoring critical metrics.

PUBLICATIONS

* indicates co-first authors

Automated Design Space Exploration in High-Level Physical Synthesis 2025

Linfeng Du, Jiawei Liang, Jason Lau, Yuze Chi, Yutong Xie, Chunyou Su, Afzal Ahmad, Zifan He, Jake Ke, Jinming Ge, Jason Cong, Wei Zhang, Licheng Guo

ICCAD '25 - The 2025 IEEE/ACM International Conference On Computer Aided Design

RapidStream IR: Infrastructure for FPGA High-Level Physical Synthesis 2024

Jason Lau, Yuanlong Xiao, Yutong Xie, Yuze Chi, Linghao Song, Shaojie Xiang, Michael Lo, Zhiru Zhang, Jason Cong, Licheng Guo

ICCAD '24 - The 43rd IEEE/ACM International Conference on Computer-Aided Design

CHARM 2.0: Composing Heterogeneous Accelerators for Deep Learning on Versal ACAP Architecture 2024

Jinming Zhuang, Jason Lau, Hanchen Ye, Zhuoping Yang, Shixin Ji, Jack Lo, Kristof Denolf, Stephen Neuendorffer, Alex Jones, Jingtong Hu, Yiyu Shi, Deming Chen, Jason Cong, Peipei Zhou

TRETS '24 - ACM Transactions on Reconfigurable Technology and Systems, Volume 17, Issue 3, Article No. 51, Pages 1 - 31

Enabling Heterogeneous Computing for Software Developers 2024

Jason Lau advised by Jason Cong

Ph.D. Dissertation, University of California, Los Angeles

TAPA: A Scalable Task-Parallel Dataflow Programming Framework for Modern FPGAs with Co-Optimization of HLS and Physical Design 2023

{Licheng Guo*, Yuze Chi*, Jason Lau*}, Linghao Song, Xingyu Tian, Moazin Khatti, Weikang Qiao, Jie Wang, Ecenur Ustun, Zhenman Fang, Zhiru Zhang, Jason Cong

TRETS '23 - ACM Transactions on Reconfigurable Technology and Systems, Volume 16, Issue 4, Article No. 63, Pages 1 - 31

RapidStream 2.0: Automated Parallel Implementation of Latency–Insensitive FPGA Designs Through Partial Reconfiguration 2023

Licheng Guo, Pongstorn Maidee, Yun Zhou, Chris Lavin, Eddie Hung, Wuxi Li, Jason Lau, Weikang Qiao, Yuze Chi, Linghao Song, Yuanlong Xiao, Alireza Kaviani, Zhiru Zhang, Jason Cong

TRETS '23 - ACM Transactions on Reconfigurable Technology and Systems, Volume 16, Issue 4, Article No. 59, Pages 1 - 30

CHARM: Composing Heterogeneous Accelerators for Matrix Multiply on Versal ACAP Architecture 2023

Jinming Zhuang, Jason Lau, Hanchen Ye, Zhuoping Yang, Yubo Du, Jack Lo, Kristof Denolf, Stephen Neuendorffer, Alex Jones, Jingtong Hu, Deming Chen, Jason Cong, Peipei Zhou

FPGA '23 - The 2023 ACM/SIGDA International Symposium on Field Programmable Gate Arrays

FPGA HLS Today: Successes, Challenges, and Opportunities 2022

Jason Cong, Jason Lau, Gai Liu, Stephen Neuendorffer, Peichen Pan, Kees Vissers, Zhiru Zhang

TRETS '22 - ACM Transactions on Reconfigurable Technology and Systems, Volume 15, Issue 4, Article No. 51, Pages 1 - 4

Sextans: A Streaming Accelerator for General-Purpose Sparse-Matrix Dense-Matrix Multiplication 2022

Linghao Song, Yuze Chi, Atefeh Sohrabizadeh, Young-kyu Choi, Jason Lau, Jason Cong

FPGA '22 - The 2022 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays

TARO: Automatic Optimization for Free-Running Kernels in FPGA High-Level Synthesis 2022

Young-kyu Choi, Yuze Chi, Jason Lau, Jason Cong

TCAD '22 - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

AutoBridge: Coupling Coarse-Grained Floorplanning and Pipelining for High-Frequency HLS Design on Multi-Die FPGAs 2021

Licheng Guo, Yuze Chi, Jie Wang, Jason Lau, Weikang Qiao, Ecenur Ustun, Zhiru Zhang, Jason Cong

FPGA '21 - The 2021 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays

TAPA: Extending High-Level Synthesis for Task-Parallel Programs 2021

Yuze Chi, Licheng Guo, Jason Lau, Young-kyu Choi, Jie Wang, Jason Cong

FCCM '21 - The 29th IEEE Annual International Symposium on Field-Programmable Custom Computing Machines

HeteroRefactor: Refactoring for Heterogeneous Computing with FPGA 2020

{Jason Lau*, Aishwarya Sivaraman*, Qian Zhang*}, Muhammad Ali Gulzar, Jason Cong, Miryung Kim

ICSE '20 - The ACM/IEEE 42nd International Conference on Software Engineering

Analysis and Optimization of the Implicit Broadcasts in FPGA HLS to Improve Maximum Frequency 2020

{Licheng Guo*, Jason Lau*}, Yuze Chi, Jie Wang, Cody Hao Yu, Zhe Chen, Zhiru Zhang, Jason Cong

DAC '20 - The 2020 57th ACM/IEEE Design Automation Conference

Hardware Acceleration of Long Read Pairwise Overlapping in Genome Sequencing 2019

{Licheng Guo*, Jason Lau*}, Zhenyuan Ruan, Peng Wei, Jason Cong
FCCM '19 - The 2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines

Reproducing Vectorization of the Tersoff Multi-Body Potential on the Intel Skylake and NVIDIA Volta Architectures 2018

Jason Lau, Yuxuan Li, Lei Xie, Qian Xie, Beichen Li, Yu Chen, Guanyu Feng, Jiping Yu, Xinjian Yu, Miao Wang, Wentao Han, Jidong Zhai
Parallel Computing, Volume 78, October 2018, Pages 47-53

KEY ENGINEERING & SYSTEMS PROJECTS

TAPA: Task-Parallel FPGA Compiler — Maintainer and Co-Author
In collaboration with lab members at UCLA, implemented TAPA, a task-parallel FPGA compiler based on Clang that enables high-level programming of FPGAs using C++ dataflow graph. Extended the compiler with nested tasks supporting complex applications. Implemented with lab members a high-performance parallel RTL co-simulation framework, allowing real-world application mixing HLS and RTL designs. Extended a high-level synthesis tool, AutoSA, to generate TAPA programs that provide higher performance than Vitis HLS.

HeteroRefactor: Source-to-Source Code Refactoring — Automated Code Refactoring Developer
Developed HeteroRefactor, a ROSE-based source-to-source code refactoring tool that automatically transforms C++ code to use heterogeneous programming models, so that the code's recursion, pointers and dynamic memory allocation are translated to vendor tool supported equivalents.

TUNA Open Source Mirror Site — Maintainer and Organizational Chair
Maintained the largest open-source mirror site in China (mirrors.tuna.tsinghua.edu.cn). Built a high-performance, reliable multi-server system with fast data storage, serving an average throughput of 3.1 Gbps used by users across China.

NGINXwise: RL-based Congestion Control — Network Software Developer
Built a production-ready NGINX-based testbed for evaluating reinforcement learning for optimizing the initial congestion control window (CWND). The testbed is used in measuring HTTP request latency on live traffic of a top Chinese website.

MPIfuse: Distributed File System — Computer System Researcher
In collaboration with team members, developed a high-performance distributed file system prototype using MPI and FUSE. Identified bottlenecks in FUSE and achieved 3.6 GB/s parallel write speeds on an 8-machine cluster, outperforming NFS on tmpfs.

CachedMIPS: FPGA-Based Processor — Hardware Design Engineer
Developed a pipelined write-back L1 cache with AHB protocol for a MIPS32r1 compatible CPU on Xilinx FPGA. Improved interrupt logic and peripheral support to enable full Linux booting in 8.4 seconds, achieving a 50x speedup on general applications.

Cherry: Cluster Management System — Full Stack Developer
Developed a network management system for a cluster used by a Chinese backbone network. Implemented deployment configuration (Puppet), resource management (virtualization, bandwidth), and metrics monitoring using Node.js, Redis, and Nagios.

iTunet: Automated Network Configuration — iOS Developer
Developed an iOS widget application that automatically configures settings for the Tsinghua University campus network. The app simplifies the process of connecting to the university's network by automating the connection setup, making the login process transparent on disconnections.

Iodine: Online Program Judge System — Full Stack Developer
In collaboration with the HUSTOJ author, developed an online judge system for programming competitions. Refactored the code to support modern web standards, including a new frontend using Bootstrap and a backend with Laravel PHP. The grading is isolated in Docker containers, allowing for secure and efficient execution of user-submitted code.

TECHNICAL SKILLS

Programming Languages: C/C++, Python, Rust, Java, JavaScript, TypeScript, Bash, Verilog.
Systems & Cloud: Linux, Docker, Kubernetes, Ansible, Ceph, Nginx, CI/CD, Distributed Systems, Multithreading, SIMD, RDMA, MPI, DevOps.
Hardware & Compilers: LLVM, MLIR, Clang, ROSE, ARM, High-Level Synthesis, FPGA, CAD, EDA, Vivado, CUDA, OpenCL, VTune, Embedded.
Web: Node.js, React, Canvas, SVG, Webpack, Django, G6.

SELECTED AWARDS

Best Paper Award	International Symposium on Field-Programmable Gate Arrays (2021)
Outstanding Contributor	Xilinx, Inc. (2021)
A. Richard Newton Young Student Fellow	Design Automation Conference (2019 & 2020)
International Champion	ASC Student Supercomputer Challenge (2017 & 2018)
National Champion	National Student Computer System Challenge (2017)
International Champion	ISC Student Cluster Competition (2017)
Dean's List	School of Engineering, HKUST (2017)
Freshman Award	Tsinghua University (2014)
National Scholarship	National Youth Science and Technology Innovation Award (2014)
National Gold Medal	National Olympiad in Informatics (2013)
International Silver Medal	Asia-Pacific Informatics Olympiad, China Region (2013)

SERVICES

- **Technical Program Committee Member** of International Conference on Field-Programmable Logic and Applications 2026
- **Technical Program Committee Member** of IEEE International Conference on Omni-Layer Intelligent Systems 2026
- **Technical Program Committee Member** of Design Automation Conference 2026
- **Technical Program Committee Member** of Great Lakes Symposium on VLSI 2026
- **Technical Program Committee Member** of IEEE International Symposium On Field-Programmable Custom Computing Machines 2026
- **Artifact Evaluation Committee Member** of IEEE International Symposium On Field-Programmable Custom Computing Machines 2026
- **Technical Program Committee Member** of International Conference on Field-Programmable Logic and Applications 2025
- **Technical Program Committee Member** of International Conference on Field-Programmable Logic and Applications 2024
- **Invited Reviewer** of Design Automation Conference 2022

REVIEWS

Reviewed **100 papers** (excluding subreviews) for:

- ACM Transactions on Architecture and Code Optimization (TACO)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Transactions on Reconfigurable Technology and Systems (TRETS)
- Design Automation Conference (DAC)
- Field-Programmable Custom Computing Machines (FCCM)
- Field-Programmable Logic and Applications (FPL)
- GigaScience
- IEEE Access

- IEEE Open Journal of Circuits and Systems (OJCAS)
- IEEE Transactions on Aerospace and Electronic Systems (TAES)
- IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computers, Special Issue (TCSI)
- IEEE Transactions on Industrial Electronics (TIE)